



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/723,261

11/26/2003

Kimmo Mylly

915-005.084

6072

4955 7590 03/20/2008

WARE FRESSOLA VAN DER SLUYS & ADOLPHSON, LLP  
BRADFORD GREEN, BUILDING 5  
755 MAIN STREET, P O BOX 224  
MONROE, CT 06468

EXAMINER

MARTINEZ, DAVID E

ART UNIT

PAPER NUMBER

2181

MAIL DATE

DELIVERY MODE

03/20/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/723,261	<b>Applicant(s)</b> MYLLY ET AL.	
	<b>Examiner</b> DAVID E. MARTINEZ	<b>Art Unit</b> 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07 December 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☒ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-9, 13-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regards to claim 1, in lines 5-6, the term “detecting in said electronic device a bus width or widths available for use in a peripheral device” renders the claim indefinite since it is not clear if the detection of the bus width is being done in the electronic device itself or if the detection of the bus width is directed to detection in the peripheral device instead.

Claim 9 recites the limitation “wherein said detecting comprises” in line 5, which renders the claim indefinite since it is not clear if it’s referring back to the detecting of a bus width (claim 1 line 2) or to the detecting of one or more indicators (claim 1 line 4).

Claim 9 also recites the limitations "said using" in line 12 and “said operating mode” in line 13. There is insufficient antecedent basis for these limitations in the claim.

Claim 13 recites the limitations "said direct indicator" in lines 1-2. There is insufficient antecedent basis for this limitations in the claim. This new rejection to claim 13 is due to the amendment of claims 11 and 12 which changed “indirect indicators” to “indirect indicator values”.

Claim 14 recites the limitations "said direct indicator" in line 3. There is insufficient antecedent basis for this limitations in the claim. This new rejection to claim 14 is due to the amendment of claims 11 and 12 which changed “indirect indicators” to “indirect indicator values”.

Art Unit: 2181

With regards to claims 2-9, due to their direct or indirect dependency from claim 1, they suffer from the same deficiencies and thus are rejected under the same rationale.

With regards to claim 15, due to its direct or indirect dependency from claims 13 or 14, it suffers from the same deficiencies and thus is rejected under the same rationale.

Due to the vagueness and a lack of clear definiteness in the claims, the claims have been treated on their merits as best understood by the examiner.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5,7-25 are rejected under 35 U.S.C. 102(b) as being anticipated by SD Memory Card Specification – Part 1 physical layer specification Version 1.01 (hereinafter “SDMCS”).

1. With regards to claims 1, SDMCS teaches a method for execution in an electronic device, comprising:

detecting in said electronic device [a host] a bus width or widths available for use [1-bit bus width or 4-bit width, deduced by detection of SPI mode or SD mode] in a peripheral device [SD Memory Card] connected to the electronic device [a host] by detecting one or more indirect indicators formed in the peripheral device [page 7 - section 3.1, page 8 last paragraph], said one or more indirect indicators being only indirectly indicative of said bus width or widths available [1-bit bus width or 4-bit width] for use in the peripheral device [page 15 section 3.3-subsections 2 and 3 below Table 1], said electronic device then

selecting a detected bus width [1-bit bus width or 4-bit width, deduced by detection of SPI mode or SD mode] from said bus width or widths detected as available for use in said peripheral device [page 4, section 1, first paragraph – a user accesses the content of the SD memory card according to an operating bus width].

2. With regards to claim 2, SDMCS teaches the method according to claim 1, wherein reference data is stored in the electronic device about at least one bus width available in the peripheral device and corresponding to one or more values of said one or more indirect indicators [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1].

3. With regards to claim 3, SDMCS teaches the method according to claim 2, wherein said one or more indirect indicators is or are indicative of information stored in the peripheral device and indicating indirectly, said bus width or widths are available in the peripheral device [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1].

4. With regards to claim 4, SDMCS teaches the method according to claim 3, wherein said indirect indicator or indicators is or are indicative of information about a clock frequency available in the peripheral device [page 6, line 9, page 17, table 3, 'Max Clock Rate'].

5. With regards to claim 5, SDMCS teaches the method according to claim 3, wherein said information is information about whether the peripheral device is fast or slow [page 17, section 3.4 – first paragraph].

6. With regards to claim 7, SDMCS teaches the method according to claim 2, comprising performing at least the following:

- transmitting a request from the electronic device to the peripheral device to transmit in return said one or more values of said indirect indicator or indicators to the

Art Unit: 2181

electronic device [page 7, section 3.1 – first paragraph, page 8 section 3.1.1 lines 10-14],

- transmitting said value or values of said indirect indicator or indicators from the peripheral device to the electronic device [page 18 lines 11-12],
- comparing said one or more values with at least one reference value from said reference data stored in the electronic device [page 18 lines 11-12] for determining the bus width or widths available for use in the peripheral device,
- selecting said one bus width available in the peripheral device [page 7, section 3.1 – first paragraph, page 8 section 3.1.1 last paragraph, page 10 last two lines] according to said identification, and
- setting the selected bus width for the peripheral device [page 7, section 3.1 – first paragraph, page 8 section 3.1.1 last paragraph, page 10 last two lines].

7. With regards to claim 8, SDMCS teaches the method according to claim 1, wherein at least one connection line is formed between the electronic device and the peripheral device, and using at least one said connection line as said indicator [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1].

8. With regards to claim 9, SDMCS teaches the method according to claim 8, comprising performing at least the following:

- initializing in said peripheral device, wherein a value of said at least one connection line is set to correspond indirectly to the bus width or widths available in the peripheral device [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1, page 18 lines 11-12],
- the electronic device detecting a state of said at least one connection line and comparing the state of said connection line with at least one reference value from

Art Unit: 2181

- said reference data stored in the electronic device [page 18 lines 11-12], followed by said
- selecting one bus width [page 7, section 3.1 – first paragraph, page 8 section 3.1.1 last paragraph, page 10 last two lines], and then
  - setting the selected bus width for the peripheral device [page 7, section 3.1 – first paragraph, page 8 section 3.1.1 last paragraph, page 10 last two lines].
9. With regards to claim 10, it is of the same scope as claim 1 and thus rejected under the same rationale.
10. With regards to claim 11, it is of the same scope as claims 1 and 2 above and thus rejected under the same rationale.
11. With regards to claim 12, it is of the same scope as claim 2 above and thus rejected under the same rationale.
12. With regards to claim 13, it is of the same scope as claim 3 above and thus rejected under the same rationale.
13. With regards to claim 14, it is of the same scope as claim 8 above and thus rejected under the same rationale.
14. With regards to claim 15 it is rejected under the same rationale as claim 2 above.
15. With regards to claim 16, it is of the same scope as claim 1 above and thus rejected under the same rationale.
16. With regards to claim 17, it is of the same scope as claim 4 above and thus rejected under the same rationale.
17. With regards to claim 18 it is of the same scope as claim 5 above and thus rejected under the same rationale.

Art Unit: 2181

18. With regards to claim 19 it is of the same scope as claim 6 above and thus rejected under the same rationale.

19. With regards to claim 20, it is of the same scope as claims 1 and 8 above and thus rejected under the same rationale.

20. With regards to claim 21, it is of the same scope as claim 1 and thus rejected under the same rationale.

21. With regards to claim 22, SDMCS teaches an electronic device [a host] comprising a bus width detector for detecting a bus width [1-bit bus width or 4-bit bus width] of a peripheral device [an SD memory card] connected to the electronic device [host in page 8 last paragraph], in which peripheral device at least one bus width is arranged to be used from a defined set of bus widths [SD mode or SPI mode each has a different bus widths once one of the modes is selected, 4-bit for SD mode and 1-bit for SPI mode] in a selected mode [SD mode or SPI mode] of the peripheral device [SD memory card], the bus width detector is configured to determine a value of one or more indirect indicators formed in the peripheral device, said one or more indirect indicators being only indirectly indicative of which bus width or bus widths is or are available for operating the peripheral device in said selected mode [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1] .

22. With regards to claim 23, SDMCS teaches the electronic device according to claim 22, wherein reference data is stored in the electronic device about at least one bus width available in the peripheral device and corresponding to said value [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1 – SD or SPI mode data references bus width data].

23. With regards to claim 24, it is of the same scope as claim 1 and thus rejected under the same rationale.



Art Unit: 2181

24. With regards to claim 25, SDMCS teaches the peripheral device according to claim 16, comprising at least one connection line, and a control unit for setting said connection line in a value which indirectly corresponds to the bus widths available in the peripheral device [page 7 - section 3.1, page 8 last paragraph, page 15 section 3.3-subsections 2 and 3 below Table 1].

Claims 1, 10, 11, 16, 21, 22, and 24, are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent Application Publication No. US 2001/0021956 A1 to Okamoto et al. (hereinafter Okamoto)

25. With regards to claims 1, 10, 11, 16, 21, 22, and 24, Okamoto teaches a method for detecting the bus width and then using a peripheral device [figs 1 element 20, fig 2 element 20a] connected to said electronic device [figs 1 and 2 - element 10], wherein at least one bus width from a determined set of bus widths is available in the peripheral device [paragraphs 57], comprising:

detecting the bus width or widths available for use in the peripheral device by detecting one or more indirect indicators formed in the peripheral device, which one or more indirect indicators is itself or are themselves only indirectly indicative of which one or ones of said set of bus widths are available for use in the peripheral device [paragraphs 8-10, 29, 54,55,57,58,59 – a mode selection is made which ultimately selects both a bus width in the peripheral card as well as a signal assignment for peripheral card pins], said electronic device then

using said peripheral device according to the detected bus width or widths [abstract – card operates in an operation mode].

Art Unit: 2181

With further regards to claim 11, Okamoto teaches wherein reference data is stored in the electronic device about at least one bus width available in the peripheral device and corresponding to said indirect indicator value [the mode available are the reference data].

Claims 1, 10, 11, 16, 21, 22, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,481,629 to Hirabayashi et al. (hereinafter Hirabayashi).

26. With regards to claims 1, 10, 11, 16, 21, 22, and 24, Hirabayashi teaches a method for detecting the bus width of and then using a peripheral device [figs 1 and 3, element 1, figs 2A and 2B] connected to an electronic device [a PC, column 4 lines 19-30], wherein at least one bus width from a determined set of bus widths is available in the peripheral device [column 4 lines 30-40, 16-bit mode and CardBus mode being a 32-bit mode], comprising:

detecting the bus width or widths available for use in the peripheral device by detecting one or more indirect indicators formed in the peripheral device are used, which one or more indirect indicators is itself or are themselves only indirectly indicative of which one or ones of said set of bus widths are available for use in the peripheral device [figs 4A and 4B, column 5 lines 15-28, column 6 lines 43-51. The level of a signal being low or high is used to recognize which operational mode the peripheral card element 1 is using. The signal conveys only a mode through a signal ultimately being a flag or bit which depending on the value, asserted or not, is checked somewhere to determine its meaning being a selection of a bus width], said electronic device then

using said peripheral device according to the detected bus width or widths [abstract – card usable according to a detected mode].

Art Unit: 2181

With further regards to claim 11, Okamoto teaches wherein reference data is stored in the electronic device about at least one bus width available in the peripheral device and corresponding to said indirect indicator value [the signal is the reference data].

***Allowable Subject Matter***

Claim 6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art alone or in combination fail to teach or fairly suggest said indicator or indicators being indicative of a version of the peripheral device.

***Response to Arguments***

Applicant's arguments filed on 12/07/07 have been fully considered but they are not persuasive.

With regards to the arguments in the remarks, pages 13-15 directed to the novelty rejection using the SDMCS reference, the Examiner respectfully disagrees.

Contrary to applicant's remarks, the determination of a communication protocol described in the SDMCS is done with indirect indication as is claimed, and no direct indication is explained by the reference. As explained by the Applicant, (page 13), the card does start in a one bit data bus by default and then the host exchanges a command to get a response from the card but the response is not "explicit information about the bus width" as Applicant alleges. The Examiner notes that Applicant's allegation that "the present invention does not require use of memory space" (page 14) is not true since the Applicant's indirect indicator relies on the deduction of the bus width after reading the version of the peripheral device which happens to be stored in memory space. Please note that this limitation is currently objected as being the

Art Unit: 2181

only allowable part of the application. Also, to clarify prior statements, the Examiner agrees that the selection of a detected bus is done *after* the bus with/widths have been indirectly determined by one or more indirect indicators which is what the prior art (SDMCS reference) teaches.

In response to Applicant's arguments in page 15 as to stating where in the prior art my conclusion is drawn as to the "if it was only shown..." statement, this conclusion is shown from SDMCS page 15 table 1 and is further explained below.

Also, as admitted by the applicant in page 9-lines 10-11 of the remarks dated 1/19/06, "a selection of a communication protocol is described", that is, the selection between one of a SD protocol mode or a SPI protocol mode. The SD protocol being one that supports a 4-bit wide bus, and the SPI protocol being one that supports a 1-bit wide bus for transfers. This selection is done after determining between the two protocol modes, the determining being indirectly indicative of two distinct bus widths since the protocol mode itself is associated with a particular bus width configuration. This is equivalent to an "indirect indication" of a bus width as is claimed by the instant application since by detecting a particular protocol mode, the system can deduce a particular bus width configuration that includes the selection of data lines and other control lines. The selection of a protocol mode ultimately indirectly selects either one of a 1-bit wide bus transfer, or a 4-bit wide bus transfer by deduction from the mode selected. The selection of the SD protocol mode or the SPI protocol mode is indirectly indicative of the bus width as well as other things such as the other pin/pad configuration that is not part of the data bus. Table 1 in page 5 of the SDMCS reference shows the signal assignment that each pin/pad of the peripheral card requires for each separate protocol mode. This signal assignment is also indirectly indicated by the selection of either one of the SD protocol mode or the SPI protocol mode. The detection of the SD protocol mode or the SPI protocol mode indirectly triggers not only the bus width selected and used for communication but also the signal assignment for each

Art Unit: 2181

pin on the peripheral card. If it was only shown that the selection of the bus width, after the determination of one of the SD protocol mode or SPI protocol mode only selected the bus width being used between the peripheral card and the host for communication, then that could be interpreted as being directly indicated, however, showing how the selection of a particular mode changes the bus width **and** the signal/pin assignment of the peripheral card, thus changing other settings other than just the bus width, leads to the conclusion that by selecting the protocol mode, additional information is used (which is stored somewhere in a memory register(s)) thus indirectly indicating the bus width, in addition to other configurations (other configurations such as the pin signal assignment of a protocol mode), for setting up of the peripheral card. In addition, the card response to the host command is indicative of a mode, and **not** of a bus width. Once the host receives the mode, it can then configure the pins as data interfaces and control interfaces depending on the received card response. Again, since the response disclosing a mode not only triggers the configuration of pins into data interfaces (bus width) but also control interfaces, the response disclosing only a mode must be indirectly indicative of the bus width.

With regards to Applicant's arguments in the remarks, page 15-16 directed to the Okamoto reference, the Examiner respectfully disagrees. Okamoto discloses storing protocol modes in an operation mode register, the protocol modes being modes that indirectly indicate a bus width associated with a particular protocol mode, in addition to pin assignment for the card and pin connection type being bidirectional, card to host, asynchronous, and/or synchronous. The different protocol modes themselves (each mode name shown being an arbitrary name), stored in the operation mode register, are associated with different bus width configurations as shown in the table of figure 6. *Again, under the same reasoning used as above for the SDMCS reference, because the configuration of each mode in table 6 of the Okamoto reference not*

Art Unit: 2181

*only does the bus width selection but also the pin assignment and pin connection type based on the reading of a register that only discloses a particular mode, the mode indirectly indicates bus widths as well as additional configuration, therefore anticipating the presently claimed invention.*

With regards to Applicant's arguments in the remarks, page 12 directed to the Hirabayashi reference, the Examiner respectfully disagrees. Hirabayashi discloses the usage of signals to detect and select a mode. The detection and selection of a mode indirectly indicates the bus width to configure. The "16-bit mode" signal indirectly indicates to configure the bus to a 16-bit wide bus, and the "CardBus" signal indirectly indicates to configure the bus to a 32-bit wide bus. It is clearly stated in column 5, lines 27-28 that detection of the operational **mode** takes place (which leads to the bus width configuration). It is not directed to the direct detection of the bus width itself. The mode signals are used to deduce the bus width configuration associated with the mode selected, therefore anticipating the presently claimed invention. This is the same reasoning used above for the SDMCS reference as well as the Okamoto reference.

### **Conclusion**

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2181

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on 571-272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DEM

/Alford W. Kindred/  
Supervisory Patent Examiner, Art Unit 2163